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Design of High speed Low Power Reversible Vedic multiplier and Reversible Divider

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ABSTRACT
This paper bring out a 32X32 bit reversible Vedic multiplier using "Urdhva Tiryakabhayam" sutra meaning vertical and crosswise, is designed using reversible logic gates, which is the first of its kind. Also in this paper we propose a new reversible unsigned division circuit. This circuit is designed using reversible components like reversible parallel adder, reversible left-shift register, reversible multiplexer, reversible n-bit register with parallel load line. The reversible vedic multiplier and reversible divider modules have been written in Verilog HDL and then synthesized and simulated using Xilinx ISE 9.2i. This reversible vedic multiplier results shows less delay and less power consumption by comparing with array multiplier.
Keywords **–** Reversible Logic Gates, Reversible Left-Shift Register, Reversible Multiplexer, Urdhva Tiryakabhayam, Vedic Multiplier

I. INTRODUCTION

Vedic mathematics is the ancient Indian system of mathematics which mainly deals with Vedic mathematical formulae and their application to various branches of mathematics. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Sri Bharati Krisna Tirtha after his research on Vedas [16]. He constructed 16 sutras and 16 upa sutras after extensive research in Atharva Veda. The most famous among these 16 are Nikhilam Sutram, Urdhva Tiryakbhayam, and Anurupye. It has been found that Urdhva Tiryakabhayam is the most efficient among these. The beauty of Vedic mathematics lies in the fact that it reduces otherwise cumbersome looking calculations in conventional mathematics to very simple ones. Reversible logic is one of the promising fjelds for future low power design technologies. Since one of the requirements of all DSP processors and other hand held devices is to minimize power dissipation multipliers with high speed and lower dissipations are critical. This paper proposes an implementation of Reversible Urdhva Tiryakabhayam Multiplier which consists of two cardinal features. One is the fast multiplication feature derived from Vedic algorithm Urdhva Tiryakabhayam and another is the reduced heat dissipation by the virtue of implementing the circuit using reversible logic gates. Also we propose a new reversible division circuit. This proposed divider is unsigned division hardware. Our proposed reversible divider composed of reversible components like reversible multiplexer, reversible PIPO left-shift register, reversible register, reversible register with parallel load line and reversible parallel adder. It is to be noted that all the scales are in the nano metric area.

II. LITERATURE SURVEY

Energy loss is an important consideration in digital circuit design. A part of this problem arises from the technological non ideality of switches and materials. The other part of the problem arises from Landauer's principle for which there is no solution. Landauer's Principle states that logical computations that are not reversible necessarily generate k*T*ln(2) joules of heat energy, where k is the Boltzmann's Constant k=1.38xl0^{-23} J/K, T is the absolute temperature at which the computation is performed. Although this amount of heat appears to be small, Moore's Law predicts exponential growth of heat generated due to information lost, which will be a noticeable amount of heat loss in next decade. Also by second law of thermodynamics any process that is reversible will not change its entropy. On thermo-dynamical grounds, the erasure of one bit of information from the mechanical degrees of a system must be accompanied by the thermalization of an amount of k*T*ln (2) joules of energy. The information entropy H can be calculated for any probability distribution. Similarly the thermodynamic entropy S refers to thermodynamic probabilities specifically. Thus gain in entropy always means loss of information, and nothing more. Design that does not result in information loss is called reversible. It naturally takes care of heat generated due to

information loss. Bennett showed that zero energy dissipation would be possible only if the network consists of reversible logic gates, Thus reversibility will become an essential property in future circuit design technologies. In previous designs the multiplier is designed using two units; one is the partial product generation unit constructed using Fredkin gates and other the summing unit constructed using 4x4 TSG gates. Also the other design presented a fault tolerant reversible 4x4 multiplier circuit. For construction of this circuit parity preserving FRG and MIG gates were used. Multiplier circuit was designed in two parts. In second part of circuit MIG gates were used instead of half adders and full adders. [7] Has proposed a design of reversible multiplier which makes use of Peres gate for generation of partial products as compared to [10], which uses Fredkin gates. For the construction of adders the HNG gate was devised. [15] Proposes low quantum cost realization of reversible multipliers which mainly uses Peres full adder gate (PF AG) for its design. It also uses Peres gates for the generation of partial products.

III. REVERSIBLE LOGIC GATES

The basic reversible logic gates encountered during the design are listed below:

3.1 Feynman Gate :It is a 2x2 gate and its logic circuit is as shown in the figure. It is also known as Controlled Not (CNOT) Gate. It has quantum cost one and is generally used for Fan Out purposes.

3.2 Peres Gate: It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost four. It is used to realize various Boolean functions such as AND, XOR.

3.3 Fredkin Gate: It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost five. It can be used to implement a Multiplexer.

3.4 HNG Gate: It is a 4x4 gate and its logic circuit is as shown in the figure. It has quantum cost six. It is used for designing ripple carry adders. It can produce both sum and carry in a single gate thus minimizing the garbage and gate counts.

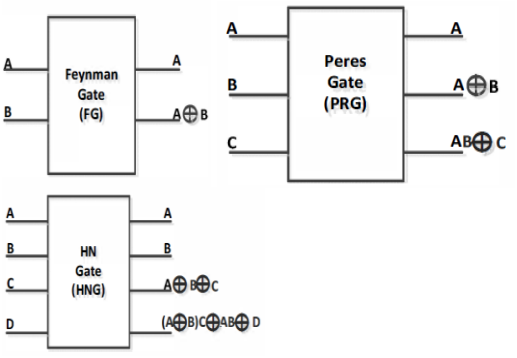


Figure1

IV. URDHVA THIRYAKABHAYAM MULTIPLICATION ALGORITHM

Urdhva Tiryakabhayam (UT) is a multiplier based on Vedic mathematical algorithms devised by ancient Indian Vedic mathematicians. Urdhva Tiryakbhayam sutra can be applied to all cases of multiplications viz. Binary, Hex and also Decimals. It is based on the concept that generation of all partial products can be done and then concurrent addition of these partial products is performed. For Example,

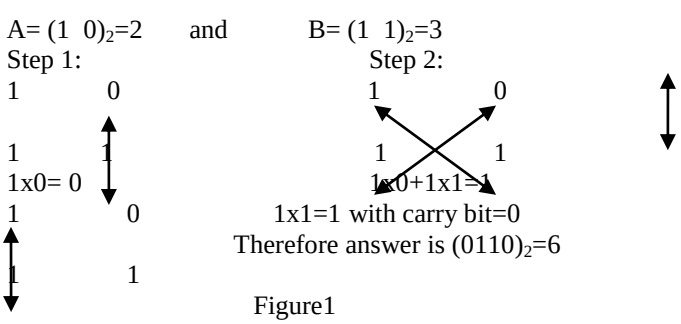
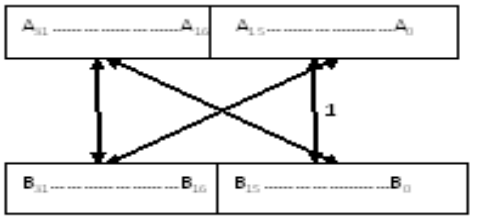


Figure1

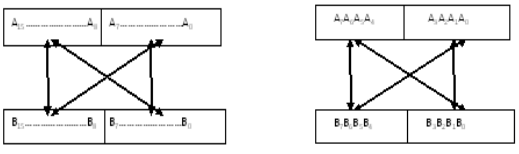
V. ARCHITECTURE OF 32X32 BIT REVERSIBLE VEDIC MULTIPLIER

The digital logic implementation of the 2X2 vedic multiplier using the reversible logic gates is as shown in figure 4. This design does not consider the fan outs. The circuit requires a total of six reversible logic gates out of which five are Peres gates and remaining one is the Feynman Gate. The quantum cost of the 2X2 vedic multiplier is enumerated to be 21. The number of garbage outputs is 9 and number of constant inputs is 4. The reversible 4X4 vedic multiplier design emanates from the 2X2 multiplier. Similarly, the reversible 8X8 vedic multiplier design emanates from the 4X4 multiplier. The reversible 16X16 vedic multiplier design emanates from the 8X8 multiplier. The reversible 32X32 vedic multiplier design emanates from the 16X16 multiplier.

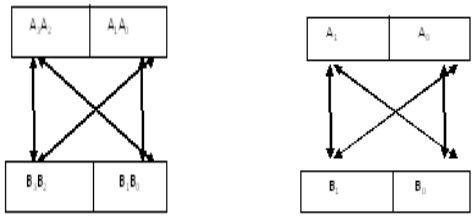
Multiplication of two 32 bit numbers will takes place in the form of following process.



32 bit is divided into two 16 bits



16 bit is divided into two 8 bits 8 bit is divided into two 4 bits



4 bit is divided into two 2 bits 2 bit UT multiplication

Figure3

The block diagram of the 32X32 Vedic Multiplier is presented in the figure 5. It consists of four 16X16 vedic multipliers each of which procures four bits as inputs; 32 bits from the multiplicand and 32 bits from the multiplier. The lower 16 bits of the output of the first 16X16 multiplier are entrapped as the lowest 16 bits of the final result of multiplication. 16 zeroes are concatenated with the upper 16 bits and given as input to the 33 bit ripple carry adder. The other 33 input bits for the ripple carry adder are obtained from the 32 bit ripple carry adder, which is obtained by summing up the outputs of other two 16x16 vedic multipliers. The lower 16 bits of output of 33 bit RCA are entrapped as next 16 bits of final result. The other 18 bits are given to next 32 bit RCA after 14 zeros are concatenated with this 18 bits. The other 32 input bits are obtained from last 16x16 vedic multiplier. The output of this 32 bit RCA will be the MSB bits of final result of multiplication which is of 64 bits. The ripple carry adder is consummated (realized) using the HNG Gate. The number of bits that need to be ripple carried verdicts the number of HNG gates to be used. Thus 32 bit ripple carry adder needs 32 HNG gates and the 33 bit adder requires 33 HNG gates.

VI. COMPONENTS REQUIRED FOR REVERSIBLE UNSIGNED DIVIDER

6.1 Reversible PIPO left-shift register: In Parallel Input- Parallel Output (PIPO) left shift register, data bits can load into the register in parallel. The properties of PIPO left-shift register have many uses in computer circuits. In division circuit, PIPO left-shift register is used and it is one of the important units in reversible division circuit. Figure 6 presents n-bit PIPO left-shift register.

6.2 Reversible multiplexer: Reversible multiplexer is shown in Figure 7. Reversible multiplexer (MUX) is realized with FRG gates. This MUX is two inputs and has one select line.

6.3 Division approaches in computer systems: For binary logic computer systems, special algorithms have been proposed to perform arithmetic tasks like multiplication and division. Multiplication in computer systems is done by repeated additions and consequently, division is done by repeated subtraction. Common algorithm used for division in computer systems is shift-subtract algorithm.

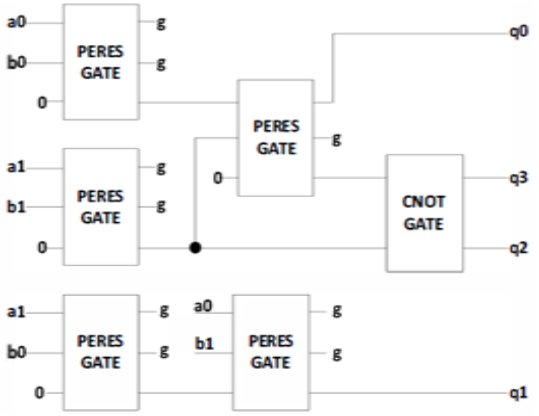


Figure4. Design of 2x2 vedic multiplier using Reversible logic gates

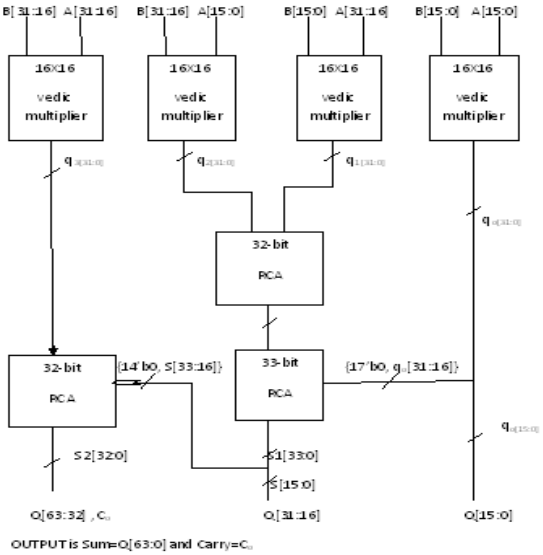


Figure5. Architecture of 32X32 bit reversible vedic multiplier

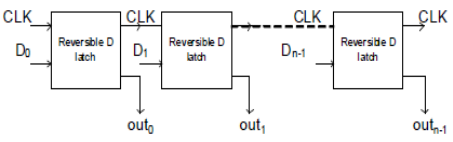


Figure6

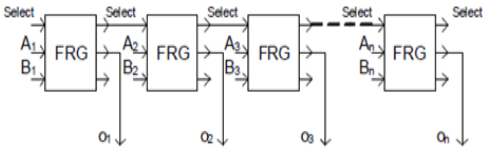


Figure7

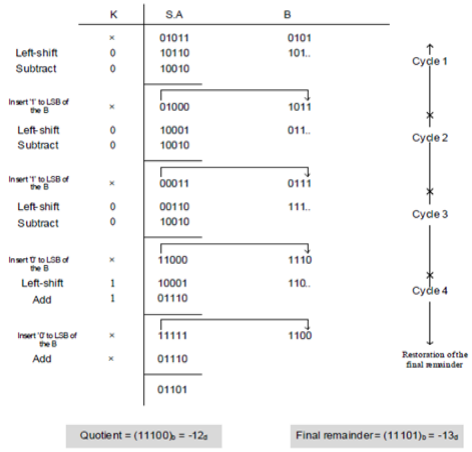


Figure8. Example for unsigned binary division

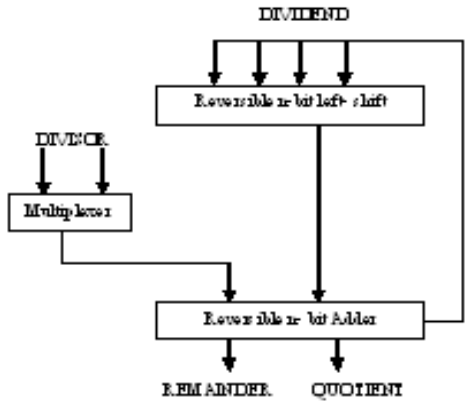


Figure9. Architecture of unsigned binary division

Figure 8 shows the binary division method in which dividend is of 8 bits and divisor is of 4 bits. Figure 9 shows the architecture for unsigned binary divisor.

VII. RESULTS

The 32x32 bit vedic multiplier is designed by using reversible logic gates like Feynman gate, Peres gate, HNG gates and four 16x16 bit vedic multipliers. Similarly divider is designed by using reversible left shit registers, multiplexers. All these modules designed in Verilog HDL and then simulated and synthesized these modules using Xilinx ISE 9.2i and shown in below figures.

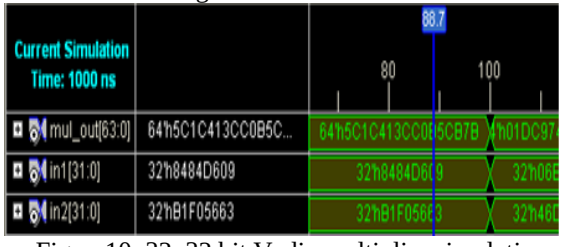


Figure10. 32x32 bit Vedic multiplier simulation result.

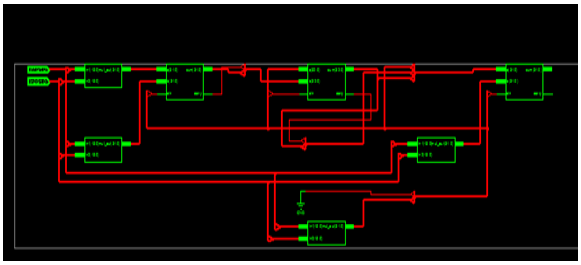


Figure11. 32x32 bit reversible Vedic multiplier RTL Schematic

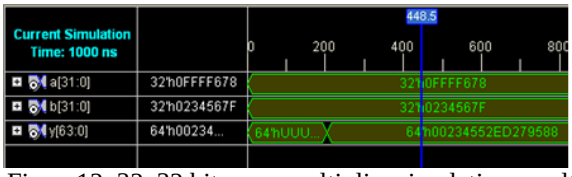


Figure12. 32x32 bit array multiplier simulation result

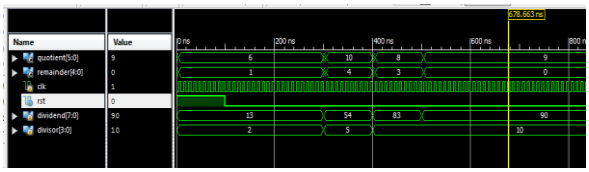


Figure13. Reversible Divider simulation result

Power consumption has been calculated for vedic multiplier and array multiplier by analyzing power in Xilinx tool and generated .ncd file. Figure 14 & Figure 15 gives total power in mW for vedic multipier and array multiplier respectively.

	Voltage (V)	Current (mA)	Power (mW)
Vccint	1.2		
Dynamic		0.03	0.03
Quiescent		25.90	31.08
Vccaux	2.5		
Dynamic		0.00	0.00
Quiescent		18.00	45.00
Vcco25	2.5		
Dynamic		3.04	7.60
Quiescent		2.00	5.00
Total Power			88.71

Figure14.32X32 bit reversible vedic multiplier power

	Voltage (V)	Current (mA)	Power (mW)
Vccint	1.2		
Dynamic		2.85	3.42
Quiescent		25.93	31.12
Vccaux	2.5		
Dynamic		0.00	0.00
Quiescent		18.00	45.00
Vcco25	2.5		
Dynamic		3.04	7.60
Quiescent		2.00	5.00
Total Power			92.14

Figure15.32x32 bit array multiplier power

sl. No	32x32 bit multiplier	Total Delay(ns)	Power consumed(mW)
1.	Vedic Multiplier	99.827ns (36.759ns logic, 63.068ns route)(36.8% logic, 63.2% route)	88.71 mW
2.	Array Multiplier	135.384ns (44.480ns logic, 90.904ns route) (32.9% logic, 67.1% route)	92.14 mW

Table1. Synthesis report

VIII. CONCLUSION

In this paper, the design of 32x32 bit Vedic multiplier and a divider is logically verified using XILINX 9.2i. The simulation results are as shown in figures 10 and 13 respectively. So based upon these results, the proposed multiplier has 35.557ns improvement in delay and 3.43 mW improvement in power, hence reversible vedic multiplier is high speed and low power multiplier.

REFERENCES

[1] Swami Bharati Krsna Tirtha, Vedic Mathematics. Delhi: Motilal Banarsidass publishers 1965
[2] Rakshith Saligram and Rakshith T.R. "*Design of Reversible Multipliers for linear filtering Applications in DSP*" International Journal of VLSI Design and Communication systems, Dec-12
[3] R. Landauer,"*Irreversibility and Heat Generation in the Computational Process*", IBM Journal of Research and Development, 5, pp.183-191, 1961.
[4] C.H. Bennett, "*Logical reversibility of Computation*", IBM J. Research and Development, pp.525-532, November 1973.
[5] R. Feynman, "*Quantum Mechanical Computers*," Optics News,Vol.1l, pp. 11-20, 1985.
[6] H. Thapliyal and M.B. Srinivas, "*Novel Reversible Multiplier Architecture Using Reversible TSG Gate*", Proc. IEEE International Conference on Computer Systems and Applications, pp. 100-103, March 20 06.
[7] Shams, M., M. Haghparast and K. Navi, Novel reversible multiplier circuit in nanotechnology. World Appl. Sci. J., 3(5): 806-810.
[8] Somayeh Babazadeh and Majid Haghparast, "*Design of a Nanometric Fault Tolerant Reversible Multiplier Circuit*" Journal of Basic and Applied Scientific Research, 2012.
[9] Thapliyal, H., M.B. Srinivas and H.R. Arabnia, 2005, A Reversible Version of 4x4 Bit Array Multiplier with Minimum Gates and Garbage Outputs, Int. Conf. Embedded System, Applications (ESA'05), Las Vegas, USA, pp: 106 114.
[10] H. Thapliyal and M.B. Srinivas, "*Reversible Multiplier Architecture Using TSG Gate*", Proc. IEEE International Conference on Computer Systems and Applications, pp. 241- 244, March 20 07.
[11] Barenco, A., C.H. Bennett, R. Cleve, D.P. Di-Vincenzo, N. Margolus, P. Shor, T. Sleator, J.A. Smolin and H. Weinfurter, 1995. Elementary gates for quantum computation. Phys. Rev. A, 52(5): 3457-3467.
[12] Bennett, C.H., 1973. Logical reversibility of computation. IBM J. Res. Dev., 17: 525-532.
[13] Feynman, R., 1985. Quantum mechanical computers.Optics News, 11: 11-20.
[14] Fredkin, E. and T. Toffoli, 1982, Conservative logic. Int. J. Theor. Phys., 21: 219-253.
[15] Haghparast, M. and K. Navi, 2008. A novel reversible BCD adder for nanotechnology based systems. Am. J. Appl., Sci., 5(3): 282-288.
[16] Haghparast, M., S.J. Jassbi, K. Navi and O. Hashemipour, 2008. Design of a novel reversible multiplier circuit using HNG gate in nanotechnology. World Appl. Sci. J., 3(6): 974-978.
[17] Haghparast, M., M. Mohammad, K. Navi and M. Eshghi, 2009. Optimized reversible multiplier circuit. J. Circuits Syst. Comp., 18(2): 311-323.
[18] Hayes, J.P., 1998. Computer Architecture and Organization. 3rd Edn., McGraw-Hill, New York. Hayes, B., 2006. Reverse engineering. Am. Sci. 94: 107-111..